REMARKS

In the Office Action of November 11, 2004, the Examiner rejected claims 1-2, 5-9, and 16-20 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,657,252 to Fried et al. ("Fried") and rejected claims 3 and 4 under 35 U.S.C. § 103(a) as being unpatentable in view of Fried.

By this Amendment, Applicants have amended claims 1 and 16 and added new claim 21. Claims 8-15 have been cancelled with prejudice or disclaimer. Claim 1 was amended to incorporate the features previously in claim 8. Claim 16 has been amended to more appropriately define the invention.

As an initial matter, Applicants note that a PTO-1449 filed with a supplemental information disclosure statement on July 26, 2004 was not returned with the Office Action. Applicants respectfully request that the Examiner consider the documents listed on the PTO-1449 file dJuly 26, 2004 and return a copy of this PTO-1449 with the next communication with the Examiner's initials indicating that these documents have been officially considered.

Claims 1-2, 5-9, and 16-20 stand rejected under 35 U.S.C. § 102(e) based on Fried. Applicants respectfully traverse this rejection.

Claim 1, as amended, is directed to a semiconductor device that includes a substrate, an insulating layer formed on the substrate, and a fin formed on the insulating layer and including a plurality of side surfaces and a top surface. The device further includes a first gate formed on the insulating layer proximate to one of the plurality of side surfaces of the fin, a second gate formed on the insulating layer separate from the first gate and proximate to another one of a plurality of side surfaces of the fin, and a protective layer formed above the fin, the first gate, and the second gate.

Additionally, a third gate is formed over the protective layer and over the fin, wherein the first, second, and third gates are independently addressable via respective gate electrodes.

Fried is directed to a FinFET having non-volatile random access memory (NVRAM) capability. (Fried, Abstract). In Fried, the "NVRAM capability arises from the presence of double floating gates arranged on and insulated from a semiconductor fin body, and a control gate arranged on an insulated from the double floating gates." (Fried, Abstract).

In contrast to Fried, claim 1, as amended, includes, among other things, a first gate formed on an insulating layer proximate to one of a plurality of side surfaces of a fin, a second gate formed on the insulating layer separate from the first gate and proximate to another one of a plurality of side surfaces of the fin, and a third gate formed over the protective layer and over the fin. The first, second, and third gates are independently addressable via respective gate electrodes.

Although Fried may disclose a FinFET with "double floating gates" and a "control gate," the double floating gates of Fried are not independently addressable via respective gate electrodes, as recited in claim 1. A floating gate, as is known in the art, is a specific type of gate that is electrically insulated (e.g., it's electrically "floating") from its surrounding structure. Fried discusses the general concept of a floating gate in the "Background of the Invention" section:

> NVRAM has been accomplished by the incorporation of a floating gate structure into the transistors of memory devices. Floating gates are comprised of conductive material which is electrically insulated from surrounding structures. A floating gate may be placed between gate insulator material and a second gate where the second gate may be a control gate. Floating gates can be charged using tunneling techniques (sometimes referred to as Fowler-Nordheim tunneling) where a large voltage is applied between the control gate and the substrate resulting in a charge accumulating in the floating gate, or another technique well known in the art, hot-electron programming. Once the floating gate has been charged, because the floating gate is electrically isolated in the circuit, that charge remains intact without the requirement of being refreshed.

(Fried, col. 1, lines 28-42) (emphasis added). The double floating gates of Fried are particularly shown by Fried as floating gates 115 and can be seen in Figures 6-11 of Fried. Floating gates 115 are clearly described by Fried, at, for example, col. 6, lines 30-46, as being electrically isolated from surrounding structures. The section of Fried states:

> As illustrated in FIG. 11, after the selective removal of portions of floating gate to expose source/drain regions of fin body 100, floating gate 115 is present within control gate 120. Floating gate 115 is isolated from control gate 120 by floating gate isolation 116 and oxide shape 102. Floating gate 115 is isolated from the substrate by the BOX 99, and insulated from the silicon which comprises fin body 100 by floating gate insulator layer 110. Therefore, floating gate 115 is electrically isolated from the surrounding structure of the semiconductor device. This electrical isolation defines the floating gate 115. Therefore, once floating gate 115 is charged, by Fowler-Nordheim tunneling or by hot-electron programming or by any other means, because there is no electrical connection between floating gate 115 and other devices and structures, the charge remains in the floating gate, making the FinFET device non-volatile. Floating gate 115 or spacer 115 may act as a capacitor buried in the device.

(Fried, col. 6, lines 30-46) (emphasis added).

Applicants submit that an isolated floating gates, as described by Fried, are clearly not independently addressable via respective gate electrodes, as recited in amended claim 1. In contradistinction, Fried provides that the floating gates are isolated, not addressable via gate electrodes.

For at least these reasons, Applicants submit that the rejection of claim 1 based on Fried is improper and should be withdrawn. The rejection of claims 2 and 5-7 under 35 U.S.C. §102(e) based on Fried should also be withdrawn, at least by virtue of the dependency of these claims from claim 1.

Claims 3 and 4 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious in view of Fried. Claims 3 and 4 depend from claim 1. Applicants submit that the rejection of these claims should be withdrawn, at least by virtue of the dependency of these claims from claim 1.

Independent claim 16 additionally stands rejected under 35 U.S.C. § 102(e) based on Fried. Claim 16, as amended, is directed to a MOSFET device that includes, among other things, a first gate material layer formed on an insulating layer and around a conductive fin; a first gate electrode connected to the first gate material and configured to allow the first gate material to be electrically biased, a second gate material layer formed over a protective layer and the conductive fin, and a second gate electrode connected to the second gate material and configured to allow the second gate material to be electrically biased independently of the first gate material. Thus, claim 16, as amended, includes first and second gate material layers and respective first and second gate electrodes connected to the gate material layers. The first gate electrode allows the first gate to be electrically biased and the second gate electrode allows the second gate to be electrically biased independently of the first gate material.

In contrast to the features of claim 16, the disclosure of Fried does not disclose or suggest first and second gate materials and first and second gate electrodes, as recited in claim 16. At most, Fried discloses a single control gate and multiple floating gates. The floating gates of Fried, however, as previously discussed, are clearly disclosed as being electrically isolated from the rest of the structure. An isolated gate could not possibly be connected to "a first gate electrode connected to the first gate material and configured to allow the first gate material to be electrically biased," as recited in claim 16, or to "a second gate electrode," as is also recited in claim 16.

Accordingly, for at least these reasons, the rejection of claim 16 is improper and should be withdrawn. Claims 17-20 depend, either directly or indirectly, from claim 16. The rejection of these claims, at least by virtue of their dependency from claim 16, should also be withdrawn. In addition, claims 17-20 recite additional features not disclosed or suggested by Fried.

Claim 19, for example, recites that the gate dielectric layers and the conductive fin break the first gate material layer into independently addressable first and second gates of the MOSFET device. The floating gates of Fried, in contrast, are isolated floating gates, and cannot be said to be independently addressable first and second gates of a MOSFET device, as recited in claim 19.

New claim 21 has been added. This claim includes features not disclosed or suggested by the cited art. For example, claim 21 recites, among other things, first, second, and third gates, and respective first, second, and third gate electrodes. For reasons similar to those discussed above with respect to claims 1 and 16, allowance of claim 21 is respectfully requested.

In view of the foregoing amendments and remarks, the applicant respectfully requests withdrawal of the outstanding rejections and the timely allowance of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: _____
Brian Ledell
Reg. No. 42,784

Date: August 27, 2004
11240 Waples Mill Road
Suite 300
Fairfax, VA 22030
Telephone: (571) 432-0800
Facsimile: (571) 432-0808